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Analysis and Optimization of Output Low-Pass Filter for Current-Source Single-Phase Grid-Connected PV Inverters

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Abstract: In this study, the design of output low-pass capacitive–inductive (CL) filters is analyzed and optimized for current-source single-phase grid-connected photovoltaic (PV) inverters. Four different CL filter configurations with varying damping resistor placements are examined, evaluating performance concerning the output current's total harmonic distortion (THD), the power factor (PF), and power losses. High-frequency harmonics are effectively attenuated by a second-order CL filter with the damping resistor placed parallel to the filter inductor. In addition, this filter type achieves the best performance by minimizing power loss. A systematic design methodology using filter normalization techniques allows to determine the optimum filter parameters based on the specified cut-off frequency (500 Hz), power loss (5% of rated power), and target THD (<5%). The analysis, simulations, and experiments show that under various operating conditions, this approach meets the grid connection standards (current THD < 5%, power factor between 0.8 leading and 0.95 lagging) while improving efficiency.

Keywords: low-pass filter; photovoltaic cells; pulse-width modulation inverters; solar power generation

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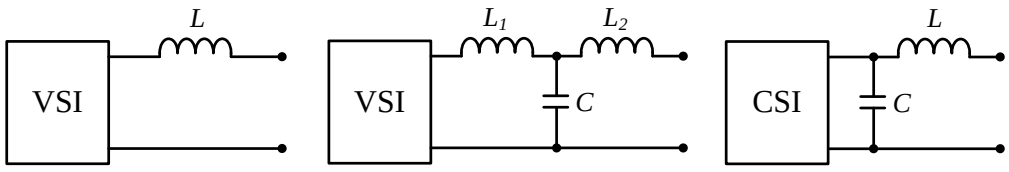
1. Introduction

The increase in the connection of renewable energy sources to power grids requires the development of efficient and reliable grid-connected inverters. An important component of these inverters is the output low-pass filters, which, apart from ensuring grid compatibility, must minimize power losses and reduce high-frequency harmonics generated by pulse-width modulation (PWM) switching. Therefore, the design of such filters requires the solution of complex problems with some trade-offs: effective harmonic attenuation must be balanced with minimizing power loss, maintaining a high power factor, and complying with grid connection standards and requirements. This paper aims to analyze and optimize output low-pass filters, specifically for current-source, single-phase grid-connected photovoltaic inverters, where the topology chosen is a second-order CL filter, studying different damping resistor placements and investigating the trade-offs involved in developing a comprehensive design methodology.

A passive low-pass filter is often used between an inverter and the grid to reduce harmonic distortion in the current fed into the grid. The configuration of the low-pass filter is decided based on the filter impedance mismatch criteria, determined by the type of inverter input, specifically, whether it is a current or voltage source [1–3]. Figure 1 presents a summary of the low-pass filter configurations. Voltage-source inverters, VSIs, represent the most common type of commercially available inverters. They typically employ either a single inductive, L, filter or an inductive–capacitive–inductive, LCL, low-pass filter. The L filter is recognized for its effectiveness in high-frequency PWM converters, primarily because of its straightforward design and common application in VSIs, as shown in recent studies [4,5]. The limitation of L-type filters is their attenuation of high frequencies at a rate of only 20 dB/decade, which restricts their application in high-powered low-frequency

converter systems [5,6]. The LCL filter solves these problems by attenuating frequencies beyond the resonant frequency by 60 dB/decade [7,8]. This results in reduced harmonic distortion at lower switching frequencies and a reduction in overall inductance, hence decreasing losses while still meeting harmonic specifications. As a result, overall costs are decreased and efficiency is increased. Studies show that LCL filters, when used with grid-connected voltage-source inverters, can provide dynamic performance comparable to traditional L filters. Designing an LCL filter is complex, requiring the consideration of current ripple, switching ripple, voltage drop, reactive power constraints, resonant frequency, and grid connection requirements [9–11]. Moreover, the LCL filter, as a third-order system, shows a resonant peak in the Bode plots. This increases the complexity of the control system [12,13].



(**a**) L type (**b**) LCL type (**c**) CL type

Figure 1. Common low-pass filter types for grid-connected inverters: The L (**a**) and LCL (**b**) filters are used to connect VSIs to the grid, while the CL (**c**) filter is designed to couple a CSI to the grid.

Figure 1b shows the LCL-type filter for VSIs. L on the inverter side is for filtering the fluctuations caused by switching, C is limited to the fundamental reactive power, and L on the grid side is for filtering the high-frequency harmonic distortions from the inverter side to the grid side [14–17]. Some methods have been developed for designing LCL filters. For example, while the trial-and-error method helps narrow down the available parameter values, it is mainly based on experience. It leads to multiple verification stages and uncertain outcomes. Even if the prerequisites are met, trial and error may not give the best result [18]. More complex filter design techniques, such as enumeration and graphical methods, are also available. These methods do not involve a complete evaluation of the damping factor [16,18,19].

LCL filters are frequently selected due to their efficient capability in attenuating harmonics. Inherent LC resonances present a challenge for LCL filters and may result in system instability if not properly managed [20,21]. Current-source inverters' CL filters exhibit a straightforward design; however, they are also susceptible to resonance problems [22]. Traditional passive damping methods, such as inserting resistors directly into the filter network, are typically used to decrease resonance; however, they frequently compromise efficiency by causing additional power losses, although this loss can be relatively small in certain applications [23,24]. The design of LCL filters usually means iterative processes that do not consistently produce optimal parameter values [24]. Moreover, the design of LCL filters often overlooks the impact of component selection on overall volume and capacitor lifetimes [25], and many existing designs focus only on internal stability, neglecting the crucial aspect of external stability due to grid interaction [26]. Such limitations have increased the search for new design methods for harmonic attenuation, power factor correction and efficiency improvement while maintaining stability.

A capacitive–inductive, CL, type filter, as seen in Figures 1c and 2, utilized with current-source inverters, attenuates frequencies at a rate of 40 dB per decade beyond its resonant frequency. Limited research has been undertaken to determine the parameters of low-pass filters for CSIs, with some studies including damping resistors, R_D, and others excluding them [27–31]. While the CL filter shows similar effectiveness, the capacitive–inductive–capacitive CLC filter is more complex, addressing similar issues associated with LCL filters in VSIs. A CLCL filter was investigated in one study; it resulted in an almost 50% reduction in THD, although there was an increase in dumping resistance losses [32].

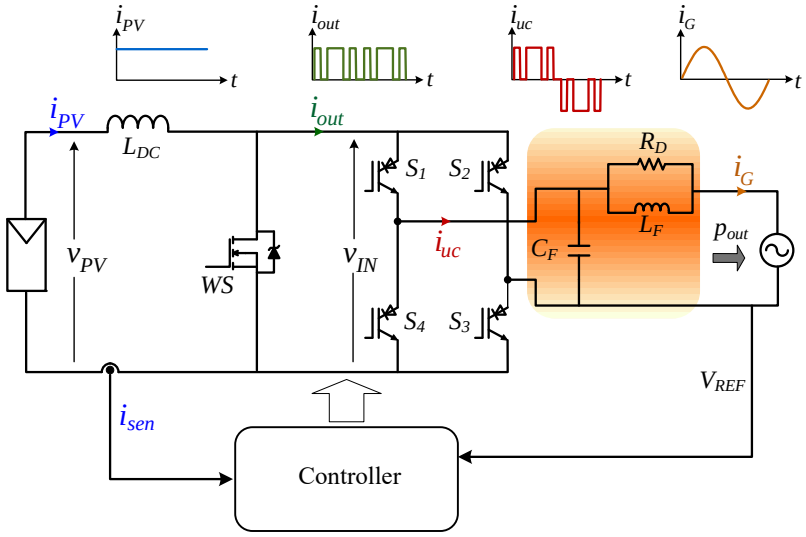


Figure 2. The current-source RB-IGBT-based single-phase grid-connected PV inverter shows waveforms for every operational phase. The output filter is configured as a parallel-damped CL type.

There are also active damping methods, which typically involve injecting an auxiliary current to counteract the resonant current, providing an alternative approach to mitigate resonance [33,34]. Active damping strategies often introduce additional complexity, cost, and potential instability issues, particularly under uncertain grid conditions [35]. Passive damping offers a simpler, more robust solution that is less sensitive to parameter variations and grid impedance uncertainties, making it a more practical choice for this application [26].

The design method presented here focuses on achieving performance targets (THD, PF, and damping resistor power losses, P_d) within certain limits for CL filters with parameter optimizations in current-source inverters. However, this is not limited to grid-connected inverter applications. The underlying principles of optimizing controller parameters for improved stability and harmonic attenuation, particularly within proportional-resonant (PR) controlled systems, are relevant to a wider range of power electronics applications. Recent studies emphasize the application of PR controllers in diverse settings, such as broadband impedance matching through digital non-Foster inspired electronics [36] and adaptive PR control for the synchronization of grid-connected inverters [37]. The techniques outlined in this paper for optimizing filter parameters to attain a specified passivity margin may be adapted and extended to improve the performance and robustness of PR-controlled systems beyond grid-connected inverters.

This study provides a systematic analysis of four different damped CL filter configurations in order to determine the most suitable filter parameters. The performance trade-offs between power losses, power factor, and THD are assessed. The study examines the effect of various damping resistor configurations on high-frequency harmonic attenuation to design a more effective and resilient filter for grid-connected photovoltaic systems.

The structure of the paper is as follows: Section 2 covers the filter resonance and damping of the CL filter, Section 2.2 describes the filter response and provides comparisons, Section 3 explains the normalization, and the analysis of THD and PF is discussed in Sections 3.2 and 3.3, Section 3.5 focuses on filter configurations, Section 4 provides an analysis of the selected filter configuration, and finally, Section 5 provides simulation and experimental waveforms for the grid-connected CSI.

Design Criteria

The main objective of a grid-connected inverter, GCI, is to deliver high-quality power with low THD to the grid while maintaining the necessary power factor. As illustrated in Figure 2, a CSI configuration with a low-pass line filter plays a critical role in this process. The properties of the low-pass filter can significantly affect the inverter's performance

regarding power factor and harmonic suppression. Consequently, careful consideration must be given to the design elements of the low-pass filter. The principal objective of constructing the low-pass filter is to guarantee that the GCI complies with required grid standards [10,11] while reducing power losses caused by damping resistance:

- From 20% to the rated output power, the power factor should be 0.8 leading and 0.95 lagging;
- It is essential to minimize high-frequency harmonics, ensuring that the output current maintains a THD of less than 5%.

These standards provide comprehensive guidelines for the grid connection of energy systems using inverters. As mentioned above, Australian Standards [11] require that inverters produce a high-quality current waveform with a power factor ranging from 0.8 leading to 0.95 lagging when the inverter output is between 20% and 100% of its rated volt-amperes. Grid-connected inverters are required to comply with specific THD standards as well [11]. The current should have less than 5% total harmonic distortion for harmonics up to and including the 50th, as indicated in Table 1. Most inverters primarily control the output current and are not required to monitor voltage harmonic distortion, although grid voltage has strict harmonic limits as well.

Table 1. Current harmonic limits [11].

Harmonic Order	Limit for Each Harmonic Based on % of Fundamental
2–9	4%
10–15	2%
16–21	1.5%
22–33	0.6%
Even harmonics	25% of equivalent odd harmonics
Total harmonic distortion (to the 50th harmonic)	5%

Additionally, losses due to iron and copper components can reduce the overall efficiency of the inverter when such a filter is employed. As a result, to keep the efficiency higher, a maximum damping resistor power loss, P_d, of 5% of the rated power is arbitrarily selected. This should also be considered in the design of a GCI low-pass filter.

2. Filter Resonance and Damping

A current-source inverter requires a specific type of filter to connect to a standard voltage-based grid (mains). This filter is known as a second-order CL-type low-pass filter. It is used to minimize the variations in electrical characteristics between the inverter and the grid, a phenomenon known as impedance mismatch [1].

As shown in Figure 2, this CL filter includes a damping resistor, represented by R_D. The filter's cutoff frequency, labeled as f_c, is the same as its resonant frequency, f_R. This is because the filter's output signal would become infinitely large at this specific frequency if there was no damping resistance. The formula for calculating the resonant frequency is given in Equation (1).

$$f_R = \frac{1}{2\,\pi\,\sqrt{L\,C}} \tag{1}$$

To avoid this potentially harmful amplification, it is crucial to make sure the filter has sufficient damping. Some damping naturally occurs due to inherent energy losses within the inductor and capacitor components. However, additional damping is often needed.

2.1. Filter Damping

In Figure 3, four potential connections for the damping resistor are illustrated. R_{D1} is placed in series with the capacitor, R_{D2} is connected in parallel with the capacitor, R_{D3} is

positioned in parallel with the inductor, and R_{D4} is arranged in series with the inductor. The third configuration was previously shown in Figure 2.

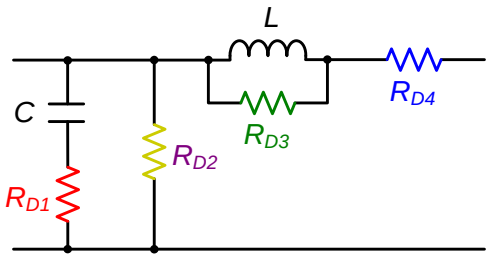


Figure 3. A low-pass filter with four damping variations, combining capacitors and inductors.

Equation (2) defines Z_0, which is determined by the filter configuration, damping resistance, and characteristic impedance. These factors together determine the quality factor. If Q is less than, equal to, or larger than 0.71 $(1/\sqrt{2})$, then the filter is classed as over–damped, critically damped, or under-damped, respectively. A switched–mode power supply filter can be constructed with a quality factor ranging from 2 to 4, even though a quality factor below 1 effectively lowers harmonic amplification [1].

$$Z_0 = \sqrt{\frac{L}{C}} \tag{2}$$

The quality factor Q is inversely proportional to damping and is associated with the filter's gain at the resonant frequency. It is important to mention that the filter gain in Figure 2 determines the output-to-input current ratio, defined as I_G/I_{UC}. The quality factor is affected by the filter topology and the specific type of damping implemented (see Figure 3). The next section continues the investigation of a variety of practical filter topologies and the associated damping techniques. The quality factor of the filter shown in Figure 2 can be represented as

$$Q = \sqrt{\left(\frac{R_D}{Z_0}\right)^2 + 1} \tag{3}$$

where the characteristic impedance of the filter is $Z_0 = \sqrt{L/C}$. When the filter's Q is too high, THD increases at its resonant frequency. If Q is too low, however, there will be significant filter loss. Grid filters are recommended to have Q values between 2 and 4 [1]. As a result, Q was initially selected as 4 for the filter analysis.

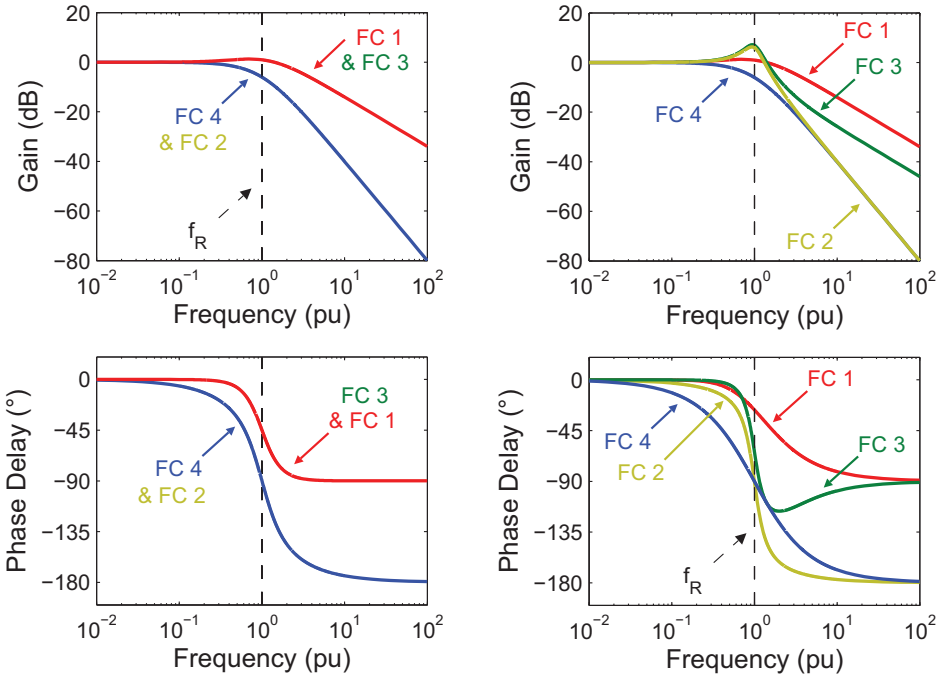
The CL filter has the capability to effectively attenuate high-frequency PWM harmonics to a significant extent (by an order of magnitude) provided that the resonant frequency is maintained at a lower value compared to the PWM switching frequency, f_{sw}. Low resonant frequencies require large filter inductance, which increases loss in the low-pass filter. Conversely, switching losses increase if the switching frequency is set too high. In this application, a f_{sw} value of 4 kHz was selected for the analysis in Section 4. This value corresponds to that used experimentally in [38,39] using the topology in Figure 2. In order to achieve a reasonable ratio of $f_c/f_{sw} = 0.125$, the value of f_c was selected as 500 Hz.

2.2. Damped Filter Response and Configuration Comparison

Figure 4 illustrates the performance of four different damped low-pass filter configurations. For two specific damping resistances, Z_0 Ω and 2 Z_0 Ω, the figures show how the gain and phase delay of the filter change as the input frequency varies. The input frequency is measured relative to the resonance frequency and plotted on a logarithmic scale from 0.01 to 100.

When the damping resistance is equal to the characteristic impedance, FC 1 and FC 3 exhibit identical gain and phase delay plots similar to FC 2 and FC 4 (Figure 4a). With an increase in damping resistance, the gain and phase delay plots exhibit distinct characteristics (see Figure 4b). FC 1 and FC 3 demonstrate similar behavior, whereas FC 2

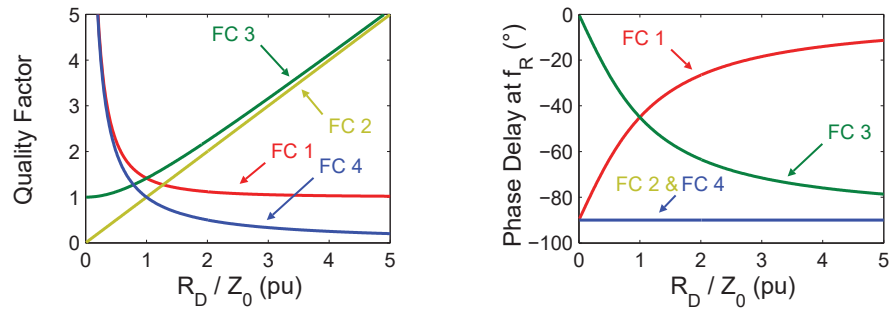
and FC 4 also show comparable characteristics. The phase delay of an nth-order low-pass filter approaches $-90\ n°$ at higher frequencies, whereas the gain generally diminishes at a rate of $-20\ n$ dB per decade. This shows that FC 1 and FC 3 behave as first-order low-pass filters, while FC 2 and FC 4 behave as second-order low-pass filters. This shows that FC 2 and FC 4 are expected to generate a lower THD than FC 1 and FC 3.



(**a**) $R_D = Z_0\ \Omega$ (**b**) $R_D = 2\ Z_0\ \Omega$

Figure 4. Analysis of the normalized gain and phase margin of a CL low-pass filter under two conditions: (**a**) $R_D = Z_0$ and (**b**) $R_D = 2\ Z_0$. FC 1 and FC 3 are first-order filters, while FC 2 and FC 4 are second-order filters. The frequency has been normalized with respect to the resonant frequency, f_R.

Figure 5 analyses the effect of damping resistance on the filter's quality factor and phase delay at resonance for various R_D values (normalized relative to the characteristic impedance, Z_0). This analysis supports the results that are presented in Figure 4. The selected filter configuration and the damping resistance both affect the Q factor and phase delay of the filter at its resonant frequency. The phase delay of FC 2 and FC 4 remains constant to the ratio of R_D to Z_0. This result suggests that in second-order designs, the required Q factor can be achieved by adjusting R_D without affecting the phase delay at resonance.



(**a**) Quality factor (**b**) Phase delay

Figure 5. Filter gain (**a**) and phase delay (**b**) at the resonant frequency, f_R, for each FC are presented based on the damping resistance, R_D. It is normalized, meaning R_D is expressed in relation to Z_0.

2.3. Filter Variables

The capacitance, inductance, and damping resistance are the three circuit parameters that comprise the filter's four variables; the filter configuration is the fourth variable. Table 2 summarizes these filter variables together with the main filter parameters they impact.

Table 2. Variables of a low-pass filter and the essential parameters they influence.

Parameter \ Variable	Resonant Frequency, f_R	Quality Factor, Q	Harmonic Attenuation	Damping Resistor Power Loss, P_d
Inductance, L	✓	✓	✓	✓
Capacitance, C	✓	✓	✓	✓
Damping resistance, R_D	✗	✓	✓	✓
Filter configuration (FC)	✗	✓	✓	✓

3. Frequency and Filter Component Normalization

Normalization is a widely recognized technique that facilitates the generalization of analyses. The cutoff frequency (or resonant frequency) and filter components are normalized. This makes the analysis much easier and makes it easy for the designer to choose component values for any system size. The representation of the normalized cutoff frequency, denoted as ω_{cn}, is associated with the base frequency, ω_B, as demonstrated in Equation (4).

$$\left.\begin{array}{l} \omega_{cn} \equiv \dfrac{\omega}{\omega_B} \end{array}\right\} \quad \text{where} \quad \omega_B = 2\pi f_1 \tag{4}$$

where the fundamental frequency of the grid (or inverter) is denoted by f_1. For a single-phase inverter that delivers rated power, P_B, to a grid with rated voltage, V_B, the base impedance, Z_B, can be calculated using Equation (5). This base impedance is then used to normalize the filter components. Essentially, the base impedance is the ratio of the base voltage, V_B, to the base current, I_B.

$$Z_B \equiv \frac{V_B}{I_B} = \frac{V_B^2}{P_B} \tag{5}$$

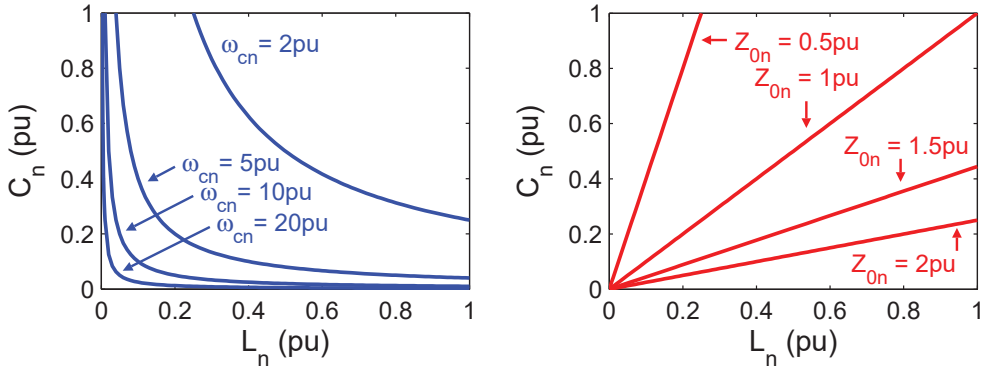
Equation (6) provides the value of the normalized filter capacitance, denoted as C_n, in terms of the base capacitance C_B. The definition of the normalized filter inductance, L_n, is defined with respect to the base inductance, L_B.

$$\left.\begin{array}{l} C_n = \dfrac{1}{w_{cn}^2 L_n} = \dfrac{C}{C_B} \\ L_n = \dfrac{1}{w_{cn}^2 C_n} = \dfrac{L}{L_B} \end{array}\right\} \quad \text{where} \quad \begin{array}{l} C_B = \dfrac{1}{\omega_B Z_B} \\ L_B = \dfrac{Z_B}{\omega_B} \end{array} \tag{6}$$

The normalized and simplified resonant frequency of the filter is represented by Equation (1). The resulting product shows an inverse relationship with the square of the filter's resonant frequency when C_n and L_n are included in this expression. The relationship is illustrated by Equation (7) and Figure 6a, showing the contours of ω_{cn} at 1, 5, 10, and 20 pu. Additionally, Figure 6b presents the contours of the normalized characteristic impedance, Z_{0n}, at 0.5, 1, 1.5, 2, and 2.5 pu, as defined by Equation (8).

$$L_n C_n = \frac{1}{\omega_{cn}^2} \tag{7}$$

$$Z_{0n} = \sqrt{\frac{L_n}{C_n}} = \frac{Z_0}{Z_B} \tag{8}$$



(**a**) Cutoff frequency, ω_{cn}, contours (**b**) Characteristic impedance, Z_{0n}, contours

Figure 6. Plots of normalized capacitance, C_n, vs. inductance, L_n, illustrating the contours for (**a**) cutoff frequency, ω_{cn}, and (**b**) characteristic impedance, Z_{0n}, contours. The contours for ω_{cn} correspond to values of 2, 5, 10, and 20 pu, while those for Z_{0n} correspond to values of 0.5, 1, 1.5, and 2 pu.

3.1. Practical Limits

Although Figure 6 shows that depending on a desired cutoff frequency or characteristic impedance, a low-pass filter can be readily designed, it should be mentioned that components could run into practical limitations, including cost, weight, size, etc. For instance, a 1 kW GCI's inductance of 0.6 pu roughly equals to 110 mH. The current rating of the inverter, specified at 4.2 A, requires an inductor that is big, bulky, and costly. Consequently, selecting a reduced value of L_n will decrease the cost, weight, and dimensions of the filter and the inverter. To achieve the same cutoff frequency, a higher capacitance would be necessary.

A higher cutoff frequency is achieved by selecting smaller values for the capacitance and inductance of the filter. In order to effectively filter out the PWM harmonics, the inverter requires a higher switching frequency, f_{sw}. Nevertheless, the inverter switching losses, P_{SW}, are directly proportional to f_{sw}. Consequently, an increase in the switching frequency yields some losses. Maximum limits are required for both switching and cutoff frequencies to reduce losses and have a decent efficiency.

For a 50 Hz GCI, a maximum switching frequency of 10 kHz (200 pu) was selected. The upper cutoff frequency depends on a number of factors. These are the filter topology, harmonic attenuation level, and inverter switching frequency. If these variables are analyzed carefully, the filter design can be optimized for efficient and effective harmonic reduction.

3.2. Harmonic Distortion and Attenuation

This section analyzes the filter's ability to reduce the overall harmonic distortion of a unipolar PWM current. Figure 7 depicts the harmonic spectrum of a 4 kHz unipolar PWM signal. The spectrum was provided by the filter gains of four different filter designs (FCs 1–4). The quality factor Q and the cutoff frequency f_c were arbitrarily selected as 1 kHz and 2, respectively. In particular, the filter gains of FC 1 and FC 3 were identical, which led to comparable THD values. Similarly, FC 2 and FC 4 showed identical gain, which resulted in identical THD.

It is clearly seen from Figure 7 that filter configurations 2 and 4 have more attenuation than those 1 and 3. Based on observations indicating a gain roll-off of -20 dB/decade, configurations 1 and 3 function as first-order filters. Configurations 2 and 4 operate as second-order low-pass filters and show a roll-off of -40 dB per decade. Factors like Q and f_c also influence filter gain, which influences the THD of the output current. Figure 8 depicts the impact of adjusting the normalized cutoff frequency, f_{cn}, on filter gain with a quality factor of 2. Figure 9 shows the effect of varying the quality factor while maintaining the cutoff frequency at 800 Hz. The PWM switching frequency of 4 kHz was used.

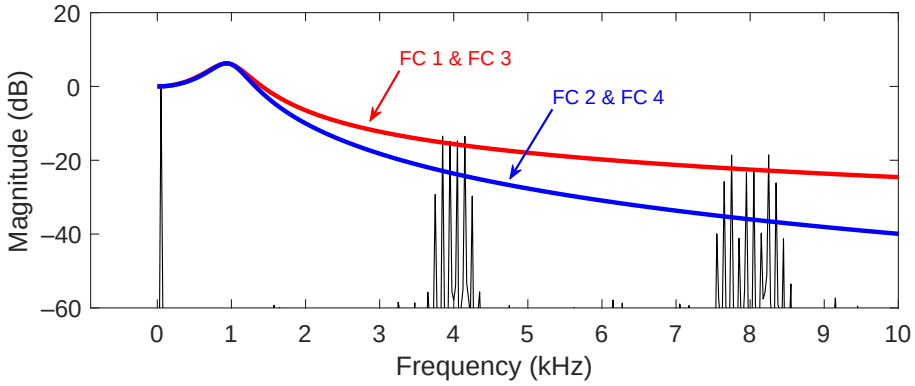
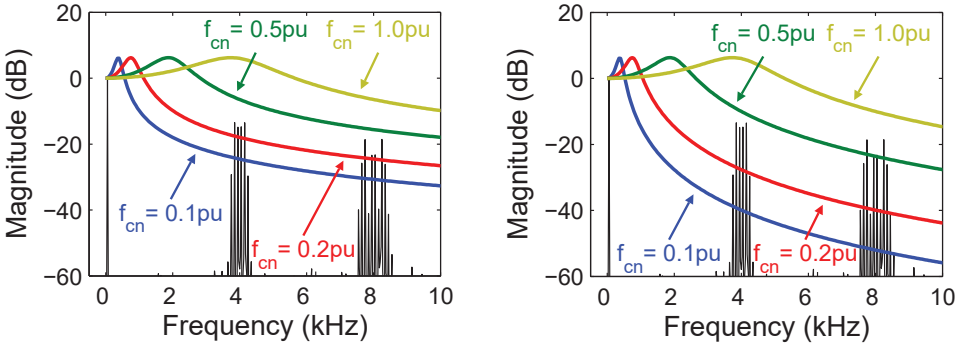


Figure 7. The unipolar PWM waveform's harmonic spectrum and the gain properties of two different filter configuration sets. FC 1 and FC 3 correspond to first-order filter responses, while configurations 2 and 4 correspond to second-order responses. Each filter is characterized by a quality factor of 2 and a cutoff frequency set at 1 kHz, with the harmonic spectrum measured at a switching frequency of 4 kHz.

Please note that in Figure 6a, the normalized cutoff frequency, denoted as ω_{cn}, is defined relative to the fundamental frequency, f_1, as shown in Equation (4). Conversely, Figures 8 and 9, utilize a normalization based on the inverter switching frequency, f_{sw}, denoted as $f_{cn} = f_c / f_{sw}$.

Figure 8 shows that when f_c approaches f_{sw}, low-pass filters become less effective, allowing higher magnitude high-frequency components to pass through and increase output current THD. Figure 9 demonstrates that the quality factor for FC 1 and FC 3 affects harmonic mitigation and consequently, THD. A low Q (around 1) leads to minimal attenuation at higher frequencies, whereas a higher Q (such as 5) considerably improves attenuation in the high-frequency range. For FC 2 and FC 4, Q has no impact on the output current's THD at low cutoff frequencies, yet its effect becomes notable as the f_c nears the switching frequency, f_{sw}.

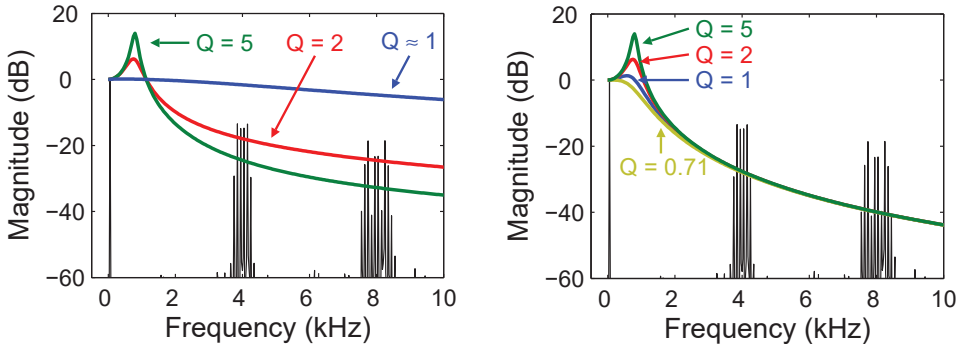


(**a**) FC 1 and FC 3 (**b**) FC 2 and FC 4

Figure 8. The analysis of the filter gain for a 4 kHz unipolar PWM harmonic spectrum shows how varying the filter cutoff frequency affects (**a**) FC 1 and FC 3 and (**b**) FC 2 and FC 4. The cutoff frequencies are normalized with respect to the switching frequency, with normalized values of 0.1, 0.2, 0.5, and 1 pu. Additionally, the PWM harmonics are now presented up to only two times the switching frequency.

Figure 10 provides the previously discussed points by illustrating the calculated THD of the output current for each filter, considering both f_c and Q. The dashed line marks the grid THD limit at 5%. The results indicate that FC 1 and FC 3 perform effectively when Q is greater than 2 and f_c is roughly between 0.2 and 0.3 pu; this finding supports Nave's recommendation of a quality factor between 2 and 4 [1]. Furthermore, the data show that the total harmonic distortion for configurations 2 and 4 remains unaffected by the quality factor when the normalized cutoff frequency, f_{cn}, is below approximately 0.3 pu.

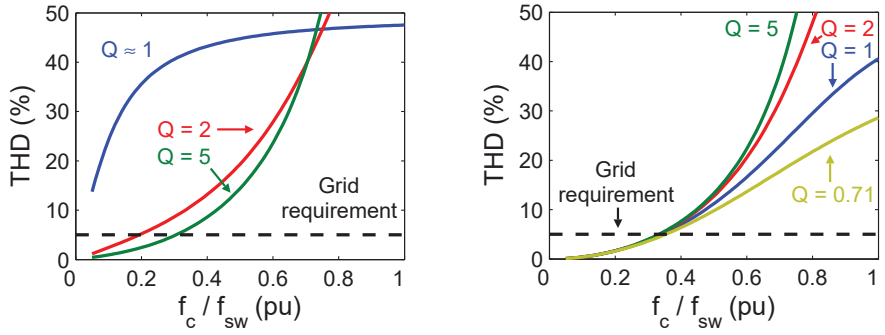
Additionally, each filter configuration meets the grid's THD requirements for a Q of 5 and a normalized cutoff frequency below approximately 0.3 pu. As a result, in order to comply with the grid's THD standards, the cutoff frequency should be limited to around 0.3 pu.



(**a**) FC 1 and FC 3 (**b**) FC 2 and FC 4

Figure 9. Filter gain for configurations (**a**) FC 1 and FC 3 and (**b**) FC 2 and FC 4, on a 4 kHz unipolar PWM harmonic spectrum, demonstrating the impact of changing the filter quality factor. For every filter design, the quality factors of 1, 2, and 5 are displayed; additionally, the critically damped case, $Q = 0.71\ (1/\sqrt{2})$, is displayed in (**b**). Note that 800 Hz is the cutoff frequency (0.2 pu, in relation to the f_{sw}).

In summary, filter configurations FC 2 and FC 4 could meet grid THD requirements over a wider range of Q and f_c than filter configurations FC 1 and FC 3. This information increases the flexibility of designing second-order low-pass filters in terms of quality factor and cutoff frequency. However, when deciding on a filter topology, the power factor and damping resistor loss should be considered.



(**a**) FC 1 and FC 3 (**b**) FC 2 and FC 4

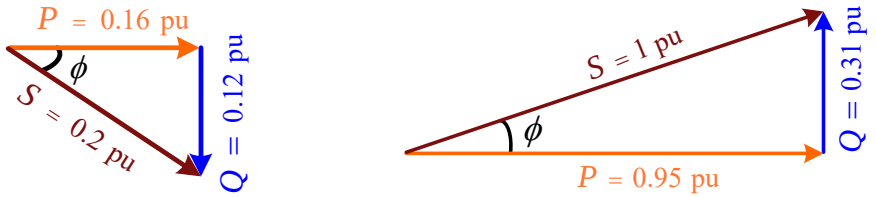
Figure 10. The relationship between the quality factor, filter cutoff frequency, and output current's THD is illustrated for configurations (**a**) FC 1 and FC 3 and (**b**) FC 2 and FC 4. The quality factors, Q, of 1, 2, and 5 are depicted in the contours for all filter configurations. The critically damped case is also present in FC 2 and FC 4, which corresponds to a quality factor of $1/\sqrt{2}$.

3.3. Power Factor Requirements

This section demonstrates how the selection of filter components affects the inverter power factor and provides guidance on determining the suitable filter inductance and capacitance to achieve the required power factor. Australian Standards define the inverter as a grid load that has to run within a power factor range of 0.8 leading to 0.95 lagging for all output apparent powers ranging from 20% to 100% of its rated capacity (0.2 to 1 pu) [11]. Table 3 and Figure 11 summarize the normalized apparent, real, and reactive powers (S, P, and Q) under these circumstances. The fundamental component of the inverter's output current is assumed to be synchronized with the grid voltage.

Table 3. Overview of normalized S, P, and Q, along with the power factor angle (ϕ), in relation to the extremes of grid power factor requirements.

Power / Grid Extremes	Apparent (S)	Real (P)	Reactive (Q)	ϕ
Power factor = 0.80 lead	0.20 pu	0.16 pu	−0.12 pu	36.9°
Power factor = 0.95 lag	1.00 pu	0.95 pu	0.31 pu	−18.2°



(**a**) Leading power factor (**b**) Lagging power factor

Figure 11. According to the grid power factor limits, the real, P, reactive, Q, and apparent power, S, triangles display (**a**) 0.8 lead and (**b**) 0.95 lag.

The reactive power in the figure above is a critical indicator of the overall reactive power exchange between the system and the grid within the specified circuit configuration. The difference between the reactive power produced by the capacitor, Q_C, and the reactive power absorbed by the inductor, Q_L, is a quantitative measurement of this reactive power. The formula for this is $Q = Q_L - Q_C$.

Figure 12 illustrates the reactive power flow within the framework of an undamped CL low-pass filter. The illustration further clarifies the dynamics of real power transfer from the inverter to the grid. It is crucial to note that the CSI does not contribute to reactive power generation. The fundamental output current is designed to operate at a unity power factor. The capacitor exclusively supplies reactive power, compensating for the demand of the inductor, while the grid absorbs that power.

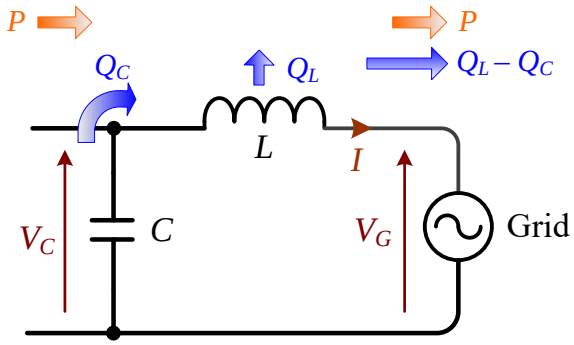


Figure 12. The real power, P, and reactive power, Q, of an undamped CL low-pass filter are displayed in the power flow diagram. The expression $Q_L - Q_C$ indicates that reactive power is either delivered or received by the grid. Additionally, the filter does not absorb real power.

The existence of a damping resistor shows that the net actual power provided to the grid is calculated as $P - P_d$, where P_d reflects the power lost in the damping resistor. Given that P_d is established at 0.05 pu (5% of rated power) at rated current, a small reduction in actual power should have a little impact on the resulting power factor. For instance, if the power factor starts at 0.95 lagging and the real power P decreases from 0.95 pu to 0.90 pu while maintaining a constant reactive power Q at 0.31 pu, the power factor slightly adjusts to 0.945 lagging.

Reactive Power

The analytical determination of the reactive power absorbed by the inductor and generated by the capacitor is presented here. Both Q_L and Q_C are represented as normalized

values. The normalized inverter output current is considered to be 1 pu for rated operation and 0.2 pu for operation at 20% of rated volt-amperes.

The inductor absorbs reactive power, Q_L, which is proportional to the square of the normalized current (I_n) and reactance, X_L. This is summarized in Equation (9), which is simplified to Equation (10). At rated current, Q_L equals L_n pu; at 20% rated power, it equals 0.04 L_n pu.

$$Q_L = I_n^2 \, X_L \tag{9}$$

$$= I_n^2 \, L_n \quad (pu) \tag{10}$$

The capacitor, denoted as Q_C, produces reactive power that is inversely proportional to the capacitive reactance, X_C, and directly proportional to the square of the capacitor voltage, V_C. This relationship is represented in Equations (11) and (12). It is important to note that $1/X_C$ can be simplified to C_n, due to the grid frequency.

$$Q_C = \frac{V_C^2}{X_C} \tag{11}$$

$$= V_{Cn}^2 \, C_n \quad (pu) \tag{12}$$

The voltage across the capacitor is the phasor sum of the grid voltage, V_G, and the voltage drop across the inductor, V_L, as described in Equation (13). This expression is simplified in Equation (14) by assuming that V_G is equal to 1 pu, and V_L can be expressed as $j \, I_n \, L_n$ ($\omega_n = 1$ pu).

$$V_C = V_G - V_L \tag{13}$$

$$= 1 - j \, I_n \, L_n \quad (pu) \tag{14}$$

3.4. Limits of Filter Components

The maximum allowable values for C_n and L_n can be established to meet power factor requirements. For a leading power factor, the maximum C_n is determined under circumstances where the inverter functions at 20% of its rated volt-amperes, which poses the most significant challenge in meeting power factor requirements. At this level, the inverter's output current is 0.2 pu, and Q is -0.12 per unit. Given that Q equals $Q_L - Q_C$, the maximum value of C_n is expressed as a function of L_n. Specifically, when the inductance is zero, to comply with the power factor requirement, the normalized capacitance must be less than 0.12 per unit. Although this maximum capacitance is expected to increase slightly with higher L_n, the increase is minimal since Q_L is equivalent to $0.04L_n$ per unit at 20% rated capacity. For instance, the leading power factor standard is met when L_n is 0.5 pu, provided $C_n \leq 0.124$ pu.

This procedure is also used in the case of a lagging power factor, where the inverter output current is set to 1 pu and the power factor is set to 0.95 (lag). To confirm compliance with the power factor requirement, the normalized capacitance is once more computed as a function of L_n. The maximum permissible inductance is 0.31 per unit without a capacitor. Introducing capacitance provides reactive power to the inductor, thereby leading to an increase in L_n. Compared to the effect of L_n on C_n in the light-load, leading power factor case, the impact of C_n on L_n under full-load conditions is more pronounced, since the voltage across the capacitor, V_C, exceeds 1 pu.

Figure 13 illustrates the limiting values of inductance and capacitance that ensure the filter meets the grid's lagging and leading power factor requirements, depicted with dashed lines. Additionally, the figure includes ω_{cn} contours at 10, 26, and 65 units per unit. The contours and dashed lines are integrated to represent two design areas, which are darkened to improve visibility. Area A, characterized by a thinner shading, corresponds to a switching frequency (f_{sw}) of 4 kHz. The wider shaded area, associated with a switching frequency of 10 kHz, includes areas A and B. Depending on the switching frequency selected, choosing

filter components within these specified regions should result in a sinusoidal output current with a fundamental frequency within the appropriate power factor range. A minimum value of ω_{cn} equal to 10 pu was selected to guarantee that the filter phase delay remains negligible. Maximum ω_{cn} values of 26 and 65 per unit were established because they corresponded to cutoff frequencies, f_{cn}, of approximately 0.33 pu, ensuring the output current waveform maintained less than 5% THD for switching frequencies of 4 kHz and 10 kHz, respectively.

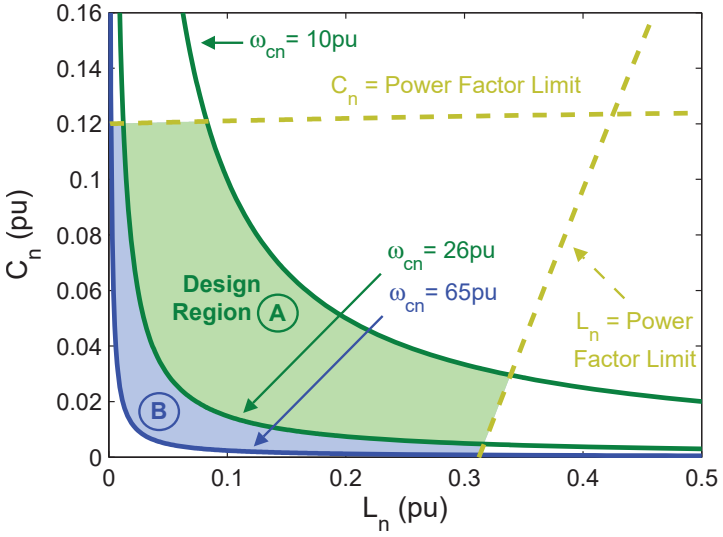


Figure 13. Normalized capacitance as a function of inductance, illustrating different cutoff frequencies and characteristic impedance values.The design region, indicated by the shaded area, limits inverter switching losses and meets specified power factor standards.

Inverter PF requirements can be met by the selection of C_n and L_n values within the designated design region. The characteristic impedance of the filter needs to be taken into account as well. The characteristic impedance, Z_{0n}, is determined by the parameters C_n and L_n, as illustrated in Equation (8). This impedance affects the selection of R_D, which in turn affects the quality factor of the filter.

As previously stated, a power factor ranging from 0.8 leading to 0.95 lagging is required for all output levels between 20% and 100% of the rated output power. The upper limit permissible for C_n at 20% output power is estimated to be 0.124 pu, derived from the requirement of a 0.8 leading power factor [10,11]. Therefore, an initial C_n value of 0.1 pu was employed for the filter shown in Figure 2 to analyze the grid-connected CSI discussed in Section 4.

3.5. Filter Configurations

The placement of the damping resistor differs among the four CL filter configurations presented in Table 4. The table presents the transfer functions $H(s)$, the quality factor Q, and the rate of high-frequency attenuation or roll-off associated with each filter configuration.

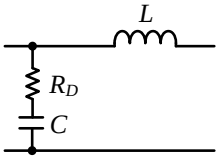
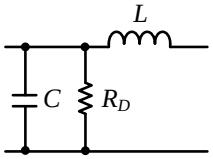
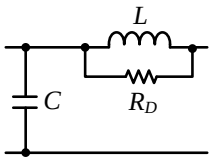
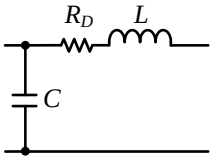
The first filter configuration utilizes a series resistor in conjunction with the capacitor of the CL filter. This arrangement leads to a first-order roll-off in the filter's high-frequency response. The filter's impedance at high frequencies is also increased. This configuration results in reasonable power dissipation P_d for the damping resistor, which primarily encounters high-frequency current components.

In FC 2, a resistor placed in parallel with the capacitor functions as a resistive load to reduce the resonant frequency of the filter. Since the full fundamental output voltage is seen across this resistor in the circuit, the high power dissipation makes this solution unacceptable.

Table 4 presents the FC 3 configuration, which incorporates a resistor functioning in parallel with the filter inductor, which causes a first-order high-frequency roll-off. The

power dissipation in R_D is expected to be considerably lower than in other types, due to the relatively small fundamental voltage drop across the inductor.

Table 4. Resistive (R_D) damping in second-order CL filter configurations [1].

FC	Circuit	Transfer Function $H(s)$	Quality Factor Q	Roll-Off Rate Beyond f_R
1		$\frac{sCR_D+1}{s^2CL+sCR_D+1}$	$\sqrt{\left(\frac{Z_0}{R_D}\right)^2+1}$	−20 dB/decade
2		$\frac{R_D}{s^2CLR_D+sL+R_D}$	$\frac{R_D}{Z_0}$	−40 dB/decade
3		$\frac{sL+R_D}{s^2CLR_D+sL+R_D}$	$\sqrt{\left(\frac{R_D}{Z_0}\right)^2+1}$	−20 dB/decade
4		$\frac{1}{s^2CL+sCR_D+1}$	$\frac{Z_0}{R_D}$	−40 dB/decade

The inductor and resistor are connected in series in filter configuration FC 4. This configuration faces two primary challenges: it results in substantial power losses and generates a resistive output impedance at lower frequencies. The impedance of the filter is similar to that of the damping resistor at low frequencies [1]. The entire grid current is passed through the resistor in series within FC 4, resulting in significant losses. It shows a second-order roll-off characteristic that is advantageous at higher frequencies.

The performance of four different CL filter configurations was thoroughly examined. The analysis was carried out with a fixed switching frequency of 4 kHz and a filter capacitance of 0.12 pu, which was considered necessary to comply with the power-factor standards. Figure 14 presents Q as a function of the normalized f_c for each FC.

The normalized cutoff frequency, which is the ratio of the cutoff frequency to the switching frequency, is shown in the picture. The contours of the graphs show the power loss and total harmonic distortion, with the solid lines indicating a constant value of 5%. The design space is divided into four distinct regions: (A) an area with total harmonic distortion below 5%, (B) a region where both THD and damping resistor power loss are below 5%, (C) a zone where power loss is under 5%, and (D) an area where both THD and power loss exceed 5%). The choice of a 5% limit for power loss was made without specific justification suggesting that a lower threshold might be more suitable for optimal design.

It can be seen in Figures 14 and 15 that the only configurations that satisfied the recommendation of having Q between 2 and 4 are FC 1 and 3 [1]. Additionally, FC 3 could meet the requirement across a broader range of cutoff frequencies and at lower Q values compared to FC 1. Moreover, the power dissipation P_d was less affected by variations in Q. On the other hand, FC 2 and FC 4 could not fulfill the required Q range; the minimum Q required for FC 4 to be in the design region is 6.5, while for FC 2 it is about 20 (for a cut-off frequency of 0.1 pu). Based on these results, FC 3 was selected as the low-pass filter for this study.

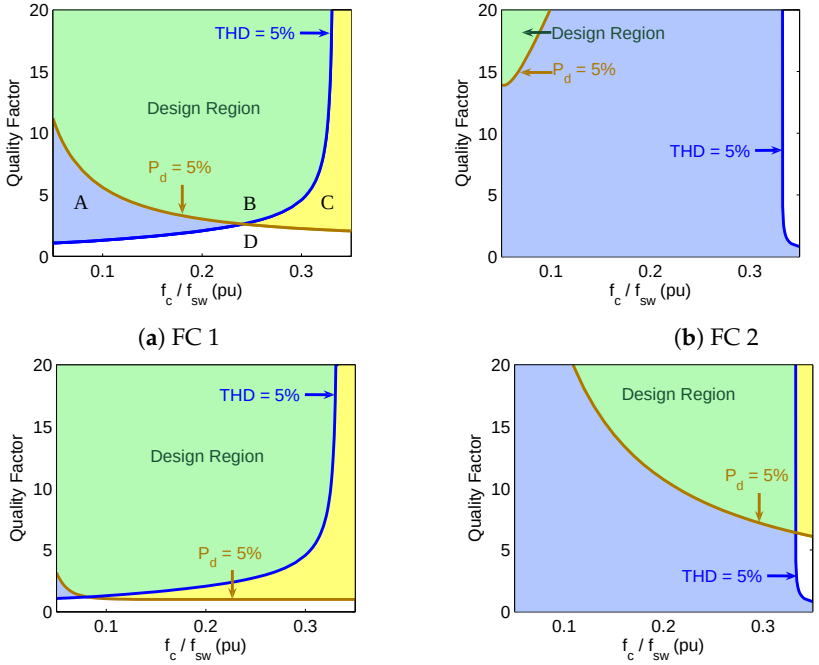


Figure 14. THD and power loss contours of 5%, for filter configurations (**a**) 1, (**b**) 2, (**c**) 3, and (**d**) 4, at a 4 kHz switching frequency.

The design region (B) in the figure is used to calculate the filter's inductance based on the cut-off frequency and filter configuration. The damping resistance can be determined using the quality factor. The inverter's performance increase if the filter's quality factor is increased. As a result, both THD and damping resistor losses would be reduced. Figure 15 shows the power loss and THD contours as 2%, 3%, 4%, and 5% for each FC. It should be noted that C_n and f_{sw} were kept constant at 0.12 pu and 4 kHz, respectively.

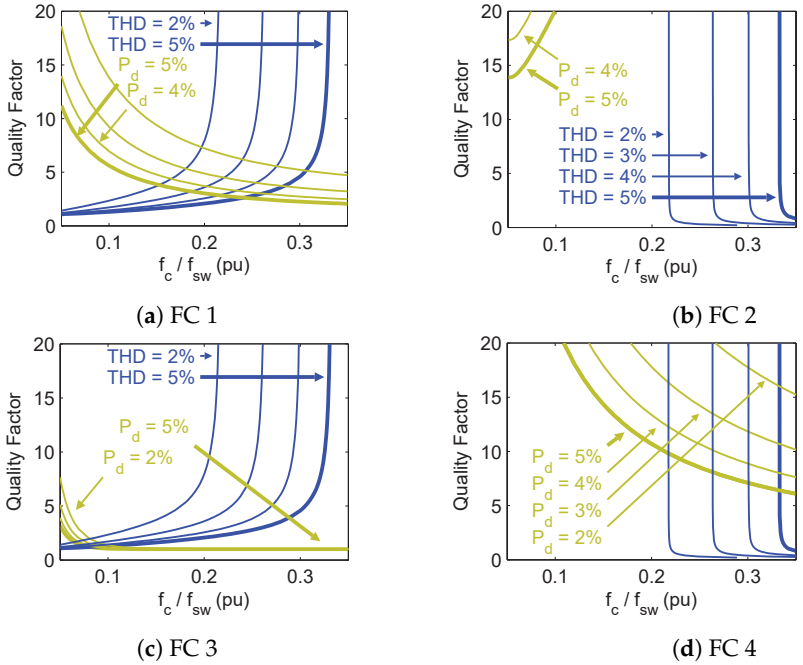


Figure 15. THD and power loss contours of 2, 3, 4, and 5%, for filter configurations (**a**) 1, (**b**) 2, (**c**) 3 and (**d**) 4, considering a capacitance of 0.12 pu and a switching frequency of 4 kHz. P_d and THD for each filter can be decreased by increasing the quality factor, with FC 3 providing the smallest variance in both Q and P_d.

4. Design Trade-Offs

Based on the analyses, the baseline filter values were determined as $C_n = 0.1$ pu, $f_c = 500$ Hz, and $Q = 4$. This filter configuration was more advantageous than the other three configurations as it was within the limits of the specified standards [10,11]. In this section, the response of the current THD, power factor, and damping resistance power loss to the variation in the baseline filter parameters are analyzed in detail to show how effective the filter configuration is. The analysis was conducted utilizing PSIM (9.1) power electronics simulation software. Figure 16 illustrates the simulation circuit. The simulation results were analyzed using MATLAB/Simulink (R2023a) software.

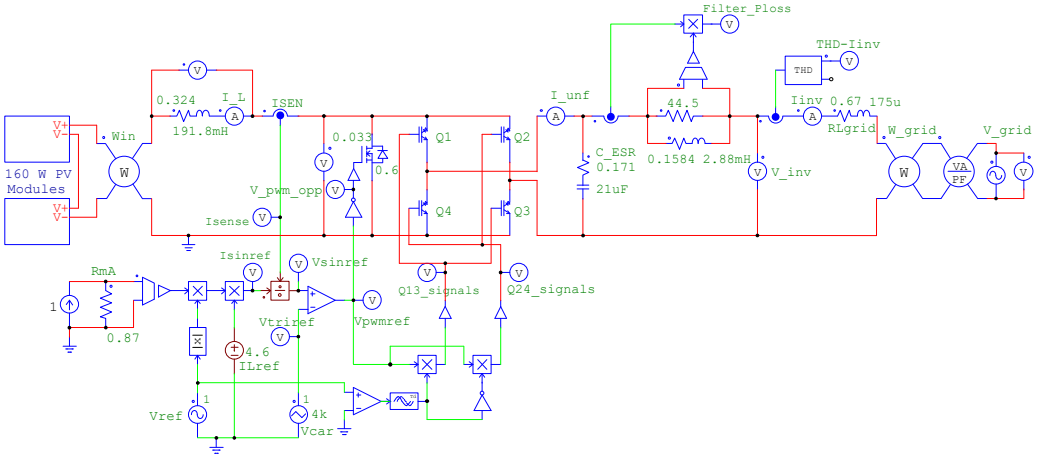


Figure 16. Inverter circuit simulation using PSIM including PV array, DC link inductor, inverter (waveshaper and unfolding circuit), low-pass output filter, grid model, and control blocks (feedforward).

In this inverter design, the photovoltaic PV array, combined with a DC link inductor, functions as a constant current source. The MOSFET switch serves as a waveform shaper, operating as a PWM current chopper, generating a waveform with a fundamental component resembling a full-wave rectified sine wave. Subsequently, the H-bridge inverter unfolds this full-wave rectified sine wave. Finally, the low-pass CL filter effectively eliminates the high-frequency components introduced by PWM to create a sinusoidal output.

4.1. Filter Design Steps

The filter design procedure is given below. The design can be realized quickly and optimally with the help of this procedure and the flow diagram in Figure 17. The filter parameters can be quickly calculated by means of the flow diagram using Equations (1)–(8). This systematic approach provides guidance for optimum filter design within the framework of specified standards.

1. Select the switching frequency for the inverter.
2. Decide which filter configuration to use.
3. Determine the normalized capacitor value to maintain the leading power factor standard ($Cn \leq 0.12$ pu).
4. Utilize the contour plot of P_d and THD vs. quality factor and cutoff frequency to establish a target for power loss and THD, ensuring THD and $P_d \leq 5\%$.
5. Calculate the value of the inductor to obtain the required cutoff frequency.
6. Calculate the damping resistance to obtain the desired quality factor.

The design methodology and simple calculation procedure, as seen in Figure 17, offer a more comprehensive approach compared to existing filter design techniques. Although trial-and-error methods can be useful for initial exploration, they lack the systematic framework for optimizing filter parameters across all relevant constraints, including those related to THD, power factor, and power loss [40]. Similarly, graphical and enumeration methods may not fully account for the complex trade-offs between different filter components

and operating conditions [16]. The proposed method, however, directly addresses these trade-offs, as evidenced by the contour plots (Figures 14 and 15) showing the relationship between filter parameters, quality factor, and performance metrics. This systematic approach offers not only efficient parameter calculation but also valuable design insights unavailable through less structured methods.

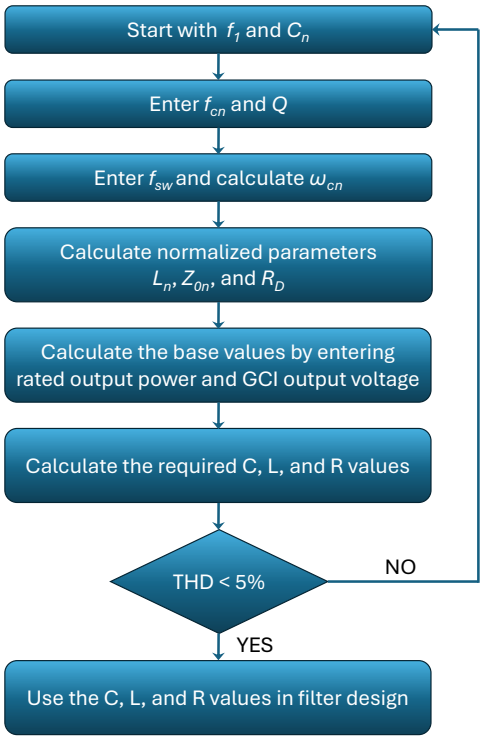
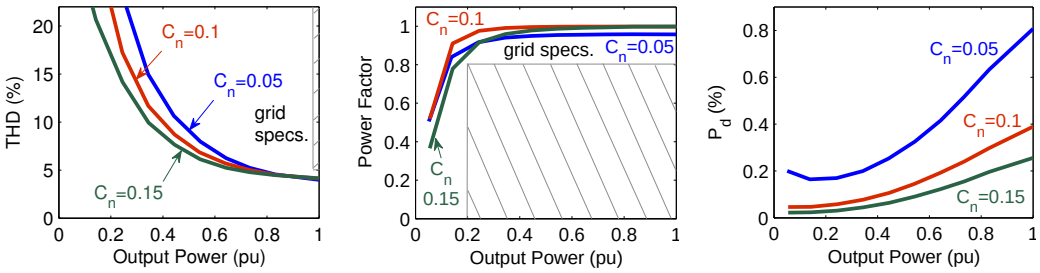


Figure 17. CL filter flowchart for determining filter parameters.

4.2. Effect of Cn Variation

The design regions shown in Figure 14 indicate a capacitance of 0.12 pu, enabling the filter to function at 20% of its rated power while achieving a 0.8 leading power factor. Furthermore, this arrangement restricts the value of L_n to a limited range, as shown in Figure 13. This limited range is advantageous as bigger capacitors are typically more economical and easier to find on the market than large inductors. The allowable range of L_n may be increased by decreasing the capacitance value C_n if required. However, it is critical to realize that this reduction would lead to an increase in Z_{0n}. This trade-off emphasizes the importance of strategically selecting component values to obtain maximum performance while balancing cost and availability. As a result, when designing the filter, it is critical to carefully analyze both capacitance and inductance values to ensure efficiency and compliance with system specifications.

Using the chosen baseline filter parameters from Section 4, Figure 18a shows how the CSI's output current's THD is related to output power for different C_n values, taking into account different levels of irradiance. Although the THD values at the rated power are similar across the different configurations, the case with a capacitance of 0.05 pu exhibits the lowest THD overall. The grid's THD requirements are met for C_n values between 0.05 and 0.15 pu at the rated output power. On the other hand, the THD shows an inverse relationship with C_n in medium to low irradiation conditions, which is especially clear in cases with smaller capacitance values. This means that under less optimal irradiation conditions, a drop in capacitance corresponds with a rise in THD.



(**a**) (**b**) (**c**)

Figure 18. The output power of the CSI varies with (**a**) output current THD, (**b**) power factor, and (**c**) damping resistance power loss (P_d) as the normalized capacitance is changed for different irradiances. Here, $Q = 4$ and $f_c = 500$ Hz.

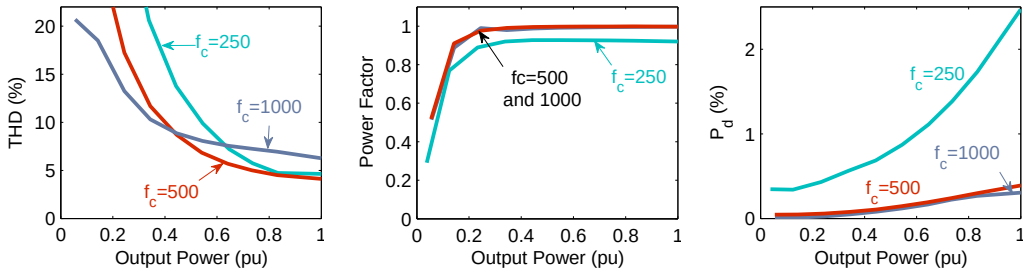
In order to maintain a consistent cutoff frequency for lower values of C_n, the corresponding value of L_n must be adjusted, which raises the characteristic impedance Z_0. As can be seen in Figure 18c, an increase in Z_0 will cause a large increase in P_d as the power dissipation P_d is directly proportional to Z_0. This relationship shows the requirement of carefully selecting capacitance and inductance values to minimize power losses and achieve higher efficiency. The increase in characteristic impedance due to higher inductance requires consideration of its effects on power dissipation, since these can affect the overal efficiency and thermal management of the system [41]. Consequently, to have a better performance and efficiency from a CL filter it is important to analyze these dynamics.

Raising the capacitance C_n to a value exceeding 0.12 pu may not ensure that the power factor remains above 0.8 when operating at 20% of the rated power, as illustrated in Figure 18b. Nevertheless, the power factor curve corresponding to C_n = 0.15 pu is close to achieving a power factor of 0.8 at that output level. The increase in the capacitance could affect the power factor. Therefore, this shows C_n should be carefully selected to operate efficiently at lower power levels. This also indicates that optimizing the parameters is very important to achieve the desired operational conditions.

4.3. Effect of fc Variation

The THD of the output current is shown in Figure19a at different levels of irradiance. The cutoff frequency f_c was set to 5, 10, and 20 times the fundamental frequency. As shown, a cutoff frequency of 250 Hz causes the inductance L_n to increase, which in turn causes the characteristic impedance Z_0 to rise. This is similar to what happened when C_n = 0.05 pu in Figure 18a. The results shown in Figure 19a suggest that the performance of the low-pass filter decreases when the f_c gets closer to the switching frequency f_{sw}. In these cases, the filter allows more high-frequency components with larger amplitudes to pass through, leading to an increase in the total harmonic distortion of the output current at the rated power. On the other hand, as the filter introduces less phase delay at higher cutoff frequencies, the harmonic content decreases. This observation is crucial since there is an inverse relationship between phase delay and the filter's cutoff frequency. Figure 19b also shows that using smaller f_c values might not meet grid needs because they cause more phase delay, even when phase advance φ is added. Therefore, adjusting the cutoff frequency not only controls the harmonic distortion but also influences the timing characteristics of the filter, impacting the overall performance and efficiency of the power system.

For the 250 Hz cutoff frequency, the power dissipation P_d is relatively high, around 3%, especially when compared to the higher cutoff frequencies shown in Figure 19c. This increased P_d is a result of the elevated Z_0 , which is a similar situation with C_n = 0.05 pu in Figure 18c. However, in this particular case, the power dissipation is noted to be doubled. This emphasizes the need for careful consideration of the cutoff frequency and the associated parameters to optimize filter performance in practical applications.

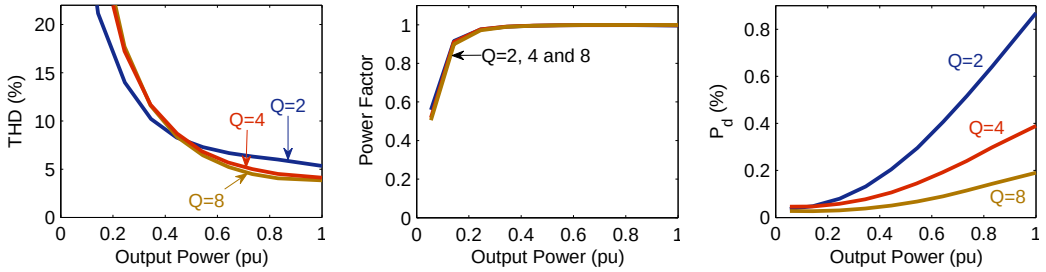


(**a**) (**b**) (**c**)

Figure 19. The CSI output power is analyzed in relation to (**a**) output current THD, (**b**) PF, and (**c**) P_d, with variations in cutoff frequency as a function of irradiance.

4.4. Effect of Q Variation

The quality factor Q of the filter varies depending on the level of irradiance, as shown in Figure 20. The THD contours in Figure 20a are quite comparable for Q values of four and eight. Even though the amplification at the cutoff frequency f_c is higher for $Q = 8$ compared to $Q = 2$ and 4, the Q of 8 achieves the lowest THD value due to its better attenuation of higher frequencies. The grid's THD requirements are just slightly exceeded by the Q = 2 case.



(**a**) (**b**) (**c**)

Figure 20. The CSI output power is analyzed in relation to (**a**) output current THD, (**b**) power factor, and (**c**) P_d, by varying the quality factor across different irradiance levels. C_n = 0.1 pu and f_c = 500 Hz.

Figure 20c shows that P_d in R_D is minimum when Q is equal to 8. However, there is a trade-off between minimising P_d and reducing THD. The decrease in P_d with increasing R_D is due to the decrease in current flowing through R_D. This is because L_n remains constant and the current decreases as R_D increases. It is also very important to note that the quality factor Q is directly proportional to the damping resistance R_D. Therefore, when Q increases, damping resistance is also increases and emphasises the relationship between these two parameters and their impact on power dissipation and system performance.

4.5. Summary of Effects of Variations

Figure 21 provides an overview of how the losses in the damping resistor vary as a function of THD under different configurations involving C_n, f_c, and Q at the rated output power P_0. When the cutoff frequency is $f_c = 1$ kHz, the system experiences the highest levels of THD. Conversely, the most significant power loss is observed when the cutoff frequency is $f_c = 250$ Hz. Among all the examined configurations, a quality factor of $Q = 8$ emerges as the most favorable design, effectively minimizing both THD and power dissipation P_d. Despite operating with a lower quality factor, the baseline filter also shows close-to-optimal performance. It performs similarly to the configuration with capacitance $C_n = 0.15$ pu at the rated output power, suggesting that careful tuning of the quality factor and cutoff frequency can substantially improve harmonic distortion and power losses. This shows the importance of optimizing these parameters to achieve efficient filter performance.

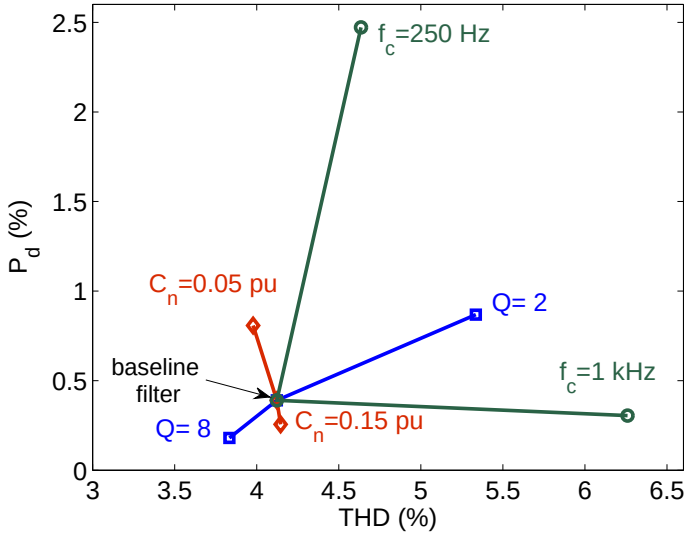


Figure 21. The power loss due to damping resistance is analyzed for various total harmonic distortion (THD) values in relation to C_n, f_c, and Q, specifically under rated output power conditions.

5. Experimental Validation of CL Filter Design

The experimental validation used two CSI prototypes (Table 5) to evaluate the effectiveness of the proposed CL filter design methodology. Prototype 1, using filter configuration FC 4 with open-loop control, showed a total harmonic distortion of 21.2% (Table 6). The comparison shows the difficulty of meeting grid standards without proper harmonic filtering and control. On the other hand, prototype 2 had 7.2% current THD with an optimized CL filter and feedforward control. This substantial THD reduction showed that an improved CL filter design with an efficient control could reduce the THD significantly even though the THD was still slightly higher than 5% Australian Standards limits [11] for the optimized filter. As a result, the performance differences among the prototypes showed the need for optimized filter design and advanced control strategies to meet the grid requirements. Future research will concentrate on integrating advanced closed-loop control to further minimize THD.

Table 5. Specifications of the two CSI prototypes.

Parameter	Prototype 1	Prototype 2
Rated maximum input power (P_0)	82 W	164 W
Input current for P_0 (I_0)	4.5 A	4.5 A
Input voltage (V_{CELL})	17.5 V	35 V
DC link inductance (L_{DC})	82 mH	192 mH
DC link inductance energy storage (E)	≈10 mJ/W	≈12 mJ/W
DC link inductor resistance (R_{LDC})	1.3 Ω	0.33 Ω
Filter inductance (L_F)	0.2–0.3 mH	2.9 mH
Filter capacitance (C_F)	100–600 µF	21 µF
Filter inductor resistance (R_L)	0.3 Ω	0.16 Ω
Filter damping resistance (R_D)	0.3–0.5 Ω	44.5 Ω
PWM switching frequency	4 kHz	4 kHz

Table 6 shows the output filter types, parameters, and current THD results for three loading conditions. The first prototype's results are compared to the second prototype. The CL filter arrangement of the first prototype exhibits series damping resistance, similar to FC 4, due to the autotransformer in the experimental setup.

Table 6. Types and parameters of inverter output filters, including quality factor, resonance frequency, and normalized capacitance. The loading configurations for three different cases and their corresponding THD values are also included.

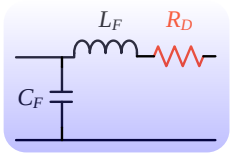
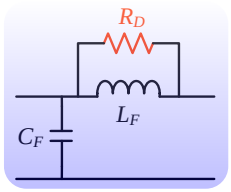
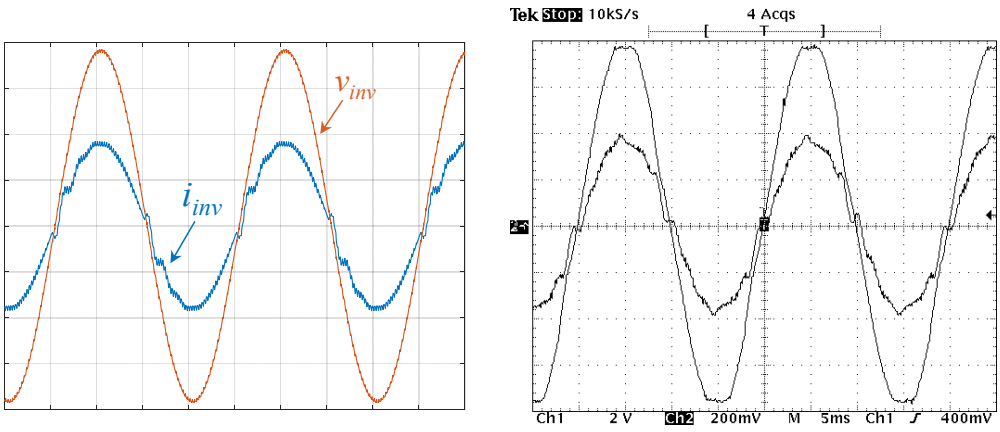
Setup	Filter	Q	f_R	C_n	Arrangement	THD
Prototype 1		2	649 Hz	0.33 pu	Resistive load Resistive + grid Grid	9.27% 16.0% 21.2%
Prototype 2		4	500 Hz	0.12 pu	Resistive load Resistive + grid Grid	3.3% 6.1% 7.2%

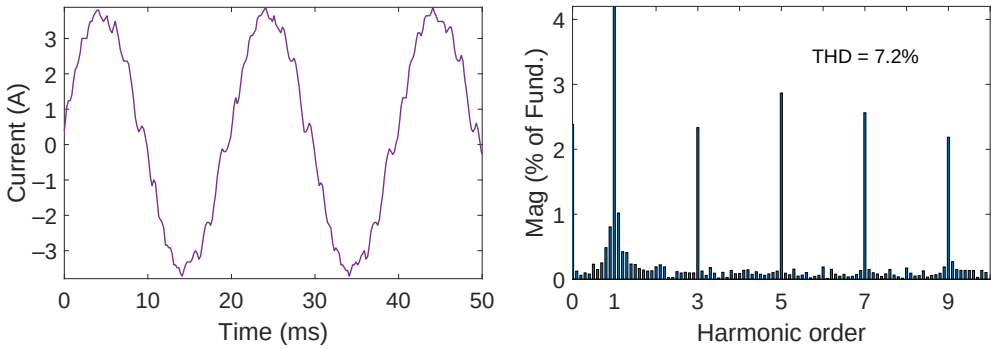
Figure 22 shows the grid-connected voltage and current waveforms. They were obtained from both simulation and experimental measurements using the optimized CL filter (configuration FC3). The simulation was validated throughout the design process by the close correlation between the simulated and measured waveforms. The low-pass output filter's phase delay caused significant components in the output current around its resonant frequency. The combination of PWM harmonics resulted in a little higher THD than the 5% limit. This can also be seen in Figure 23.

Figure 23 shows some harmonic distortion present in the output current of the CSI with the optimized CL filter, which used the baseline filter parameters. Open-loop control yielded a total harmonic distortion of 8.1% (see Figure 22), considerably exceeding the grid connection requirement limit of 5% with the pure grid connection. Despite the use of feedforward control, THD was still higher than permitted at 7.2%. This shows that effective harmonic filtering requires a robust closed-loop control strategy. This study focused on the optimization of the CL filter design through the use of a damping resistor. The design technique can be used with several control algorithms, including the PR control described in Section 1. As a result, this CL filter design method tries to reduce total harmonic distortion while additionally reducing losses and ensuring grid compliance.



(**a**) Simulation (**b**) Measurement

Figure 22. Grid-connected inverter's output voltage and current (**a**) simulation (**b**) measurement. The output filter configuration is FC 3. The parameters can be seen in Tables 5 and 6. The vertical and horizontal scales are 2 A, 20 V, and 5 ms per division.



(**a**) Output current (**b**) FFT spectrum

Figure 23. Measurment of the (**a**) output current with its (**b**) FFT spectrum. The output filter configuration is FC 3.

6. Conclusions

The high-frequency PWM harmonics generated by a current-source grid-connected inverter are eliminated by a capacitive–inductive low-pass grid filter, designed based on impedance mismatch criteria. The analysis of this filter indicates that incorporating damping is crucial to mitigate the effects of resonance. This study explored four different configurations for placing the damping resistor and investigated the corresponding trade-offs involved between power loss and harmonic attenuation, focusing on the THD of the output current. The optimal design, which efficiently minimized power loss while attenuating high-frequency PWM harmonics, was identified as the configuration where the damping resistor was placed in parallel with the filter inductor. Furthermore, the study highlighted that selecting the filter's capacitance and inductance required balancing between the grid's power factor and the cutoff frequency, demonstrating the importance of strategic component selection in optimizing filter performance and ensuring effective harmonic suppression.

A detailed filter design procedure was developed to determine the filter parameters according to the specified cutoff frequency, power loss, and optimal output current THD. Baseline values for the filter parameters were set to $C_n = 0.1$ pu, $f_c = 500$ Hz, and $Q = 4$. This filter was used to analyze the impact of a non-linear PV array current on the CSI output. Parameter optimization occurred within defined limitations. The analysis revealed that a low cutoff frequency ($f_c \leq 250$ Hz) may not meet the grid's THD and PF requirements. Additionally, a low quality factor ($Q < 2$) and a high capacitance value ($C_n > 0.15$ pu) may not meet grid standards for THD and PF. The designed low-pass filter met the grid's THD and PF requirements while producing less power loss.

Using two prototypes, the experiments confirmed that the design approach was practically effective. The power factor consistently remained within acceptable limits. The THD results showed a significant reduction; however, they slightly exceeded the 5% limit as defined in [11]. This shows that the inverter system will need an improved control algorithm in parallel with the CL filter design procedure to maintain the THD standard while maintaining efficiency. Despite this limitation, the CL filter design methodology presented in this study offers a structured approach for efficiently determining and implementing into practice the ideal values of the inductance (L), capacitance (C), and damping resistance (R_D).

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Abbreviations

The following abbreviations are used in this manuscript:

CL	Capacitive–inductive low-pass filter
CLC	Capacitive–inductive–capacitive low-pass filter
CSI	Current-source inverter
FC	Filter configuration
GCI	Grid-connected inverter
L	Inductive low-pass filter
LC	Inductive–capacitive low-pass filter
LCL	Inductive–capacitive–inductive low-pass filter
PF	Power factor
PV	Photovoltaic
RB-IGBT	Reverse Blocking Insulated Gate Bipolar Transistor
PWM	Pulse-width modulation
THD	Total harmonic distortion
VSI	Voltage-source inverter

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